IN THE CLAIMS

Following are the current claims. For the claims that have **NOT** been amended in this response, any differences in the claims below and the current state of the claims is unintentional and in the nature of a typographical error:

1. (Currently Amended) A Content Addressable Memory ("CAM") architecture providing improved speed, comprising:

an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving ~~the~~ compare-data and for reading and/or writing data in the array of CAM cells respectively;

outputs of ~~the~~ said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation; and

a control logic for implementing search and address decoding operations during a first state and enabling read-or-write operation[[s]] within a second state of the same clock cycle in the event of a match.

2. (Previously Presented) The CAM architecture as claimed in claim 1, wherein the control logic comprising a sequencing circuit that enables data comparators of the CAM cell array and an address decoder of read/write block during the first state of the clock and enables the read-or-write operation in the second state of the same clock.

3. (Currently Amended) A method for improving speed of a Content Addressable Memory ("CAM") architecture in steps of:

connecting an array of CAM cells to a compare-data-write-driver and to a read/write block, for receiving ~~the~~ compare-data and for reading and writing data in the CAM cell respectively;

coupling a match block to said array of CAM cells providing match outputs signal lines for identifying a match/no-match at the end of a [[S]]search operation;

performing the search and address decoding operations during a first state of the clock cycle; and

implementing the read/write operation after a successful search during a second state of the same clock cycle.

4. (Previously Presented) A content addressable memory device, comprising:

a content addressable memory core, having a plurality of data lines, a plurality of word line address inputs, and a plurality of comparison result outputs;

a compare data write driver, coupled to the plurality of data lines of the content addressable memory core, capable of providing data for comparison in a compare operation;

a read/write block, coupled to the plurality of data lines and the plurality of word line address inputs of the content addressable memory core, capable of

decoding a word line address of a cell of the content addressable memory core, and

one of writing data from the data lines to the addressed cell in a write operation and reading data from the addressed cell to the data lines in a read operation; and

a control block, coupled to the compare data write driver and the read/write block, capable of

causing the compare data write driver and the content addressable memory core to perform a compare operation, and

causing the read/write block to decode a word line address and to perform one of a write operation and a read operation,

wherein the control block

causes a compare operation and a decoding of a word line address to be performed during a first state of a first clock cycle, and

causes one of a write operation and a read operation to be performed during a second state of the first clock cycle.

5. (Previously Presented) The content addressable memory device of Claim 4, wherein the control block causes the read/write block to partially decode a word line address during the first state of the first clock cycle and to complete decoding of the word line address during the second state of the first clock cycle.

6. (Previously Presented) The content addressable memory device of Claim 4, wherein the control block causes the read/write block to decode a word line address and to perform one of a write operation and a read operation during a second clock cycle, without causing the compare data write driver and the content addressable memory core to perform a compare operation during the second clock cycle.

7. (Previously Presented) The content addressable memory device of Claim 4, wherein the control block causes the compare data write driver and the content addressable memory core to perform a compare operation during a second clock cycle, without causing the read/write block to perform one of a write operation and a read operation during the second clock cycle.

8. (Previously Presented) The content addressable memory device of Claim 4, further comprising a match block, coupled to the comparison result outputs of the content addressable memory core, comprising a match output signal indicating whether a match was found during a compare operation.

9. (Previously Presented) The content addressable memory device of Claim 8, wherein the control block causes the one of a write operation or read operation to be performed in the second state of the first clock cycle only if a match is found in the compare operation performed during the first state of the first clock cycle.

10. (Previously Presented) For use in a content addressable memory device, a method of performing both a compare operation and one of a write operation and a read operation on the content addressable memory device in a single clock cycle, the method comprising the steps of:

during a first state of a first clock cycle

causing the content addressable memory device to perform a compare operation, and

decoding a word line address of a cell of the content addressable memory device; and

during a second state of the first clock cycle, one of writing data to the addressed cell and reading data from the addressed cell.

11. (Previously Presented) The method of Claim 10, wherein the step of decoding the word line address is partially performed during the first state of the first clock cycle and is completed during the second state of the first clock cycle.

12. (Previously Presented) The method of Claim 10, further comprising the steps of:

during a second clock cycle

decoding a word line address of a cell of the content addressable memory device, and

one of writing data to the addressed cell and reading data from the addressed cell,

wherein the content addressable memory device is not caused to perform a compare operation during the second clock cycle.

13. (Previously Presented) The method of Claim 10, further comprising the step of causing the content addressable memory device to perform a compare operation during a second clock cycle, wherein data is neither written to nor read from the content addressable memory device during the second clock cycle.

14. (Previously Presented) The method of Claim 10, further comprising the step of generating a match signal indicating whether a match was found during the compare operation.

15. (Previously Presented) The method of Claim 14, wherein the one of writing data to the addressed cell and reading data from the addressed cell during the second state of the first clock cycle is performed only if a match was found during the compare operation performed during the first state of the first clock cycle.

16. (Previously Presented) A data processing apparatus, comprising:

a content addressable memory core having a plurality of data lines, a plurality of word line address inputs, and a plurality of comparison result outputs;

a compare data write driver, coupled to the plurality of data lines of the content addressable memory core, capable of providing data for comparison in a compare operation;

a read/write block, coupled to an address bus, data input and output connections, the plurality of data lines, and the plurality of word line address inputs of the content addressable memory core, capable of

decoding a word line address of a cell of the content addressable memory core from a signal on the address bus, and

one of

loading data on the data input connection and writing the loaded data to the addressed cell in a write operation, and

sensing data from the addressed cell on the data lines and latching the sensed data to the data output connection in a read operation; and

a control block, coupled to the compare data write driver and the read/write block, capable of

causing the compare data write driver and the content addressable memory core to perform a compare operation, and

causing the read/write block to decode a word line address and to perform one of a write operation and a read operation,

wherein the control block

causes a compare operation and a decoding of a word line address to be performed during a first state of a first clock cycle, and

causes one of a write operation and a read operation to be performed during a second state of the first clock cycle.

17. (Previously Presented) The data processing apparatus of Claim 16, wherein the control block causes the read/write block to decode a word line address and to perform one of a write operation and a read operation during a second clock cycle, without causing the compare data write driver and the content addressable memory core to perform a compare operation during the second clock cycle.

18. (Previously Presented) The data processing apparatus of Claim 16, wherein the control block causes the compare data write driver and the content addressable memory core to perform a compare operation during a second clock cycle, without causing the read/write block to perform one of a write operation and a read operation during the second clock cycle.

19. (Previously Presented) The data processing apparatus of Claim 16, further comprising a match block, coupled to the comparison result outputs of the content addressable memory core, comprising a match output signal indicating whether a match was found during a compare operation.

20. (Previously Presented) The data processing apparatus of Claim 19, wherein the control block causes the one of a write operation or read operation to be performed in the second state of the first clock cycle only if a match is found in the compare operation performed during the first state of the first clock cycle.